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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/763,204	02/20/2001	Fabien Clermidy	034299-311	3428

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2184	9

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/763,204	Applicant(s) CLERMIDY ET AL.	
	Examiner Yolanda Wilson	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-6* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chean et al. in view of Khotimsky et al. (USPN 6646989B1). As appears in claim 1, Chean et al. discloses a step of positioning the functional elements of the logic network on page 62 and see Figure 9 on page 62, "Direct reconfiguration (DR) is a simple scheme that is the basis for the family of fault-stealing techniques. It uses one row and one column of spares (R=C=1)."

Chean et al. fails to explicitly state a routing step of programming interconnecting elements on the physical network by choosing a maximum number of interconnecting elements which can be passed between two neighboring processors using a shortest track search algorithm.

Khotimsky et al. discloses this limitation in column 2, lines 5-9, "Well-known methods, such as Dijkstra's shortest path algorithm, have been developed, which given

the single static view of the network, determine under fairly general conditions the shortest routing path between any two network nodes."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a routing step of programming interconnecting elements on the physical network by choosing a maximum number of interconnecting elements which can be passed between two neighboring processors using a shortest track search algorithm. A person of ordinary skill in the art would have been motivated to have a routing step of programming interconnecting elements on the physical network by choosing a maximum number of interconnecting elements which can be passed between two neighboring processors using a shortest track search algorithm because finding the shortest track search algorithm is a well known routing algorithm for finding the shortest path between nodes on a network.

3. As per claim 2, Chean et al. discloses a network functional element positioning sequence which is composed of a starting functional element and a sequence of functional elements including all functional elements is determined on page 62 and see Figure 9 on page 62, "Direct reconfiguration (DR) is a simple scheme that is the basis for the family of fault-stealing techniques. It uses one row and one column of spares (R=C=1)."

Chean et al. discloses for each of the functional elements it is positioned tentatively starting with its logical position then if required in case of failure in each of the positions located at a distance 1, distance 2... from the logical position of this functional element a restriction being that one and only one spare position is to be used

with respect to the possible positions of previously positioned functional elements stopping when S+1 positions have been tested S being the number of spare functional elements; if S+1 positions have been tested without success returning to the previous functional element in the positioning sequence and proceeding with the next position for this functional element on page 62, 2nd,3rd and 4th paragraphs, "Fault – stealing techniques... In DR, a faulty cell (i,j) can be shifted right to a fault-free cell (i,j+1) or down to (i+1,j). The set consisting of cells (i,j), (i,j+1), and (i+1,j) is referred to as an 'adjacency domain'."

4. As per claim 4, Chean et al. discloses the starting functional element is the top left functional element the following functional elements are the functional elements to the right and below the starting functional element and so on following a diagonal on page 62 and see Figure 9 on page 62, "Direct reconfiguration (DR) is a simple scheme that is the basis for the family of fault-stealing techniques. It uses one row and one column of spares (R=C=1)."

5. As per claim 5, Chean et al. discloses the network is divided into functional element blocks and a block positioning sequence is defined starting with a starting block and going through all the blocks from one neighboring block to the next the possible positions for the functional elements of one block not including any logical position of the functional elements of previously positioned blocks on page 62, "The fixed-stealing algorithm scans all rows in the order of increasing index numbers. In each row, the rightmost unavailable cell is shifted right and other faulty cells 'steal' (are vertically shifted to) available cells on the next row."

6. As per claim 6, Chean et al. discloses the functional elements are processors on page 58, "A fault-tolerant processor array... is a two-dimensional array of identical and regularly interconnected processing elements (PEs) incorporating redundant circuitry (spares) and hardware for reconfiguration. A cell is a processing element of an FTPA... There are many variants of processor-array architectures. For example, processing elements can be as complex as a modern microprocessor or as simple as an arithmetic logic unit."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ROBERT BEAUSOLIEL
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TECHNOLOGY CENTER 2100